REMARKS

Pending Claims

Claims 1 and 6 are pending. Claims 1 and 6 have been amended. Claims 2-4 have been canceled without prejudice or disclaimer. No new matter has been added.

Claim Rejections Under 35 U.S.C. §112

Claims 1-4 and 6 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants have amended independent claims 1 and 6 to clarify that which the applicants regard as the invention. In particular, Applicants use the term "restrictions" in a manner consistent with the description in the Specification on page 15, lines 5-18 in which it is stated that restrictions are imposed on program descriptions which define a plurality of devices by employing a Java program language.

In particular, each of claims 1 and 6 set forth program descriptions which define a plurality of devices by employing a Java program language. Restrictions to the Java language descriptions are imposed in the program descriptions that define devices on a single bus which use a run method of the Java program language. The claims have been amended to set forth that the method imposes an inhibition of dynamic instantiation restriction and an inhibition of a start method call from the run method restriction on the program descriptions by employing a Java program language.

According to the Specification, the model of a system to-be-designed is designed by descriptions based on the Java language. Each device on a single bus is described using the

"run( ) method" of the Java language. In the "run( ) method", program codes which are to be executed in a thread constituting a multi-thread are described within the parentheses ( ). A clock is expressed using barrier synchronization. In general, the "barrier synchronization" is a synchronization technique which employs waiting for all data which should be processed at the same time, in the case of receiving data from a plurality of modules. *See* page 13, lines 1-13. The restriction that imposes inhibition of dynamic instantiation pertains to the process alteration. *See* page 15, lines 13-15 of the Specification, for example.

The inhibition of a start method call from the run method restriction that is imposed on the program descriptions by employing a Java programming language relates to verification of the bus protocol which involves modeling of the bus operations of the devices on a single bus. *See* page 15, lines 13-18 of the Specification, for example. Accordingly, the claims are definite and understood to one having ordinary skill in the art of Java program language, and therefore the rejection under 35 U.S.C. §112, second paragraph, should be withdrawn.

Claim Rejections Under 35 U.S.C. §103

Claims 1-4 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bowen, U.S. Patent No. 6,691,301, in view of Panchul et al, U.S. Patent Publication No. 2001/0034876, further in view of Hines, U.S. Patent Publication No. 2005/0246682.

Applicants request reconsideration of the rejections in view of the foregoing amendments and for the following reasons.

Claims 1 and 6 have been amended. Claims 2-4 have been canceled without prejudice

or disclaimer. In particular, claims 1 and 6 are directed to the system development method and data processing system of the invention. As amended, each claim sets forth that the intermediate expression is a member selected from the group consisting of a concurrent control flow flag, a temporal automaton with a concurrent parameter, or a temporal automaton with parameters. The amendment additionally sets forth parametric model checking as performed for the parameter generation and the real-time restriction is given by RPCTL. As amended, the claims are patentable over Bowen, Panchul and Hines, whether each reference is considered individually or in combination.

In particular, Bowen is relied upon for disclosing a C-like programming language to generate logic hardware enabling the compilation of programs into synchronous hardware thereby compiling high level algorithms directly into gate level hardware. Specifically, Bowen discloses using Handel-C which allows one to use a high-level language to program FPGAs. Bowen further discloses that a clock and clock speed may be assigned for working with the simple but explicit model of one clock cycle per assignment. *See* column 10, lines 5-8 of Bowen. However, Bowen does not disclose inputting program descriptions which define a plurality of devices by employing a Java program language capable of describing parallel operations.

Applicants note that Bowen discloses an interface adjustment inspection in co-simulation with HDL. *See* column 83, lines 15-59 of Bowen. On the other hand, parametric model checking that is performed according to the embodiments of the present invention is for parameter generation. Additionally, in the embodiments of the present invention, real-time restriction given by RPCTL is claimed whereas in Bowen it is merely explained that

time adjustment and co-simulation is desired.

Panchul describes the facilitation of the design of an actual hardware implementation for digital circuits using a high-level programming language, such as Java. Panchul does not disclose inputting program descriptions as set forth in the independent claims, as amended, wherein the inhibition of dynamic instantiation restriction and the inhibition of a start method call from the run method restriction are imposed on the program descriptions by employing Java program language. Accordingly, Panchul does not make up for the deficiencies in Bowen with respect to the invention as set forth in claims 1 and 6.

Hines is relied upon for disclosing the incorporating of barrier synchronizations in order to enforce synchronization of activities. However, Hines is directed to behavioral automata in which time can be directly described. *See* paragraphs 649-673, for example. On the other hand, in the claimed invention, the input program descriptions are converted into intermediate expressions that are one of a control flow flag, a temporal automaton with a concurrent parameter and a temporal automaton with parameters. In this manner, according to the embodiments of the invention, the progress of time can be clearly described. Further, although Hines is relied upon for disclosing the constraint equation of a propositional logic level (*see* paragraphs 198 – 205), Hines does not disclose real-time restrictions given by RPCTL as claimed by applicants.

Claims 1 and 6 are patentable over Bowen, Panchul and Hines, whether considered individually or in combination, and therefore the rejection under 35 U.S.C. §103(a) should be withdrawn.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

Mattingly & Malur, P.C.

John R. Mattingly
Registration No. 30,293
703/684-1120

Date: May 19, 2009